Product/Process Change Notice - PCN 20_0142 Rev. -

Analog Devices, Inc. Three Technology Way Norwood, Massachusetts 02062-9106

This notice is to inform you of a change that will be made to certain ADI products (see Appendix A) that you may have purchased in the last 2 years. **Any inquiries or requests with this PCN (additional data or samples) must be sent to ADI within 30 days of publication date.** ADI contact information is listed below.

PCN Title: ADTR1107 Data Sheet Limit Correction

Publication Date: 19-Feb-2020

Effectivity Date: 19-Feb-2020 *(the earliest date that a customer could expect to receive changed material)*

Revision Description:
Initial Release.

Description Of Change:

Revise the VDD_LNA voltage limits:

From: MIN 3.3 V, Typical 5.0, MAX 5.5 V
To: MIN 2.0 V, Typical 3.3 V, MAX 3.6V

Reason For Change:

The data sheet is being changed to reflect the correct operating voltage range for VDD_LNA.

Impact of the change (positive or negative) on fit, form, function & reliability:

The change has no impact of fit form or functionality of the device.

Product Identification *(this section will describe how to identify the changed material)*

Product data sheet correction only. There is no change to product design.

Summary of Supporting Information:

Data sheet ADTR1107 REV A, Table 4, Page 5 will reflect the VDD_LNA correction. See attached data sheet specification comparison.

Supporting Documents

Attachment 1: Type: Revised Datasheet Specification

ADI_PCN_20_0142_Rev_-_ADTR1107_Spec Comparision.pdf

For questions on this PCN, please send an email to the regional contacts below or contact your local ADI sales representatives.			
Americas:	**Europe:**	**Japan:**	**Rest of Asia:**
PCN_Americas@analog.com	PCN_Europe@analog.com	PCN_Japan@analog.com	PCN_ROA@analog.com

Appendix A - Affected ADI Models				
Added Parts On This Revision - Product Family / Model Number (3)				
ADTR1107 / ADTR1107ACCZ	ADTR1107 / ADTR1107ACCZ-R7	ADTR1107 / ADTR1107XCCZ		

Appendix B - Revision History			
Rev	**Publish Date**	**Effectivity Date**	**Rev Description**
Rev. -	19-Feb-2020	19-Feb-2020	Initial Release.

Receive state, self biased, VDD_LNA = 3.3 V, VGG_LNA = 0 V, VDD_SW = 3.3 V, VSS_SW = −3.3 V, CTRL_SW = 3.3 V, transmit state off, T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
OVERALL FUNCTION						
Frequency Range		14		18	GHz	
RECEIVE STATE						
Small Signal Gain		16	18		dB	ANT to RX_OUT
Gain Flatness			±0.9		dB	
Input Return Loss			13		dB	ANT to RX_OUT
Output Return Loss			18		dB	ANT to RX_OUT
OP1dB		12	14		dBm	ANT to RX_OUT
P_{SAT}			16.5		dBm	ANT to RX_OUT
OIP3			25.5		dBm	ANT to RX_OUT P_{OUT} per tone = 0 dBm
Noise Figure			3		dB	ANT to RX_OUT
Isolation						
ANT to TX_IN			26		dB	Transmit state off
RX_OUT to TX_IN			46		dB	Transmit state off
RF Settling Time						
0.1 dB			17		ns	50% CTRL_SW to 0.1 dB of final RF output
0.05 dB			22		ns	50% CTRL_SW to 0.05 dB of final RF output
Switching Speed						
Rise and Fall Time	t_{RISE}, t_{FALL}		2		ns	10% to 90% of RF output
Turn On and Turn Off Time	t_{ON}, t_{OFF}		10		ns	50% CTRL_SW to 90% of RF output
VDD_LNA		3.3	5.0	5.5	V	
I_{DQ}_LNA			80		mA	Self biased

SPDT switch bias at VDD_SW = 3.3 V, VSS_SW = −3.3 V.

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT						VDD_SW and VSS_SW
Positive	IDD_SW		14		µA	
Negative	ISS_SW		120		µA	
DIGITAL CONTROL INPUTS						CTRL_SW
Voltage						
Low		0		0.8	V	
High		1.2		3.3	V	
Current (Low and High)			<1		µA	

Receive state, self biased, VDD_LNA = 3.3 V, VGG_LNA = 0 V, VDD_SW = 3.3 V, VSS_SW = −3.3 V, CTRL_SW = 3.3 V, transmit state off, T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
OVERALL FUNCTION						
Frequency Range		14		18	GHz	
RECEIVE STATE						
Small Signal Gain		16	18		dB	ANT to RX_OUT
Gain Flatness			±0.9		dB	
Input Return Loss			13		dB	ANT to RX_OUT
Output Return Loss			18		dB	ANT to RX_OUT
OP1dB		12	14		dBm	ANT to RX_OUT
P_{SAT}			16.5		dBm	ANT to RX_OUT
OIP3			25.5		dBm	ANT to RX_OUT P_{OUT} per tone = 0 dBm
Noise Figure			3		dB	ANT to RX_OUT
Isolation						
ANT to TX_IN			26		dB	Transmit state off
RX_OUT to TX_IN			46		dB	Transmit state off
RF Settling Time						
0.1 dB			17		ns	50% CTRL_SW to 0.1 dB of final RF output
0.05 dB			22		ns	50% CTRL_SW to 0.05 dB of final RF output
Switching Speed						
Rise and Fall Time	t_{RISE}, t_{FALL}		2		ns	10% to 90% of RF output
Turn On and Turn Off Time	t_{ON}, t_{OFF}		10		ns	50% CTRL_SW to 90% of RF output
VDD_LNA		2.0	3.3	3.6	V	
I_{DQ}_LNA			80		mA	Self biased

SPDT switch bias at VDD_SW = 3.3 V, VSS_SW = −3.3 V.

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT						VDD_SW and VSS_SW
Positive	IDD_SW		14		µA	
Negative	ISS_SW		120		µA	
DIGITAL CONTROL INPUTS						CTRL_SW
Voltage						
Low		0		0.8	V	
High		1.2		3.3	V	
Current (Low and High)			<1		µA	